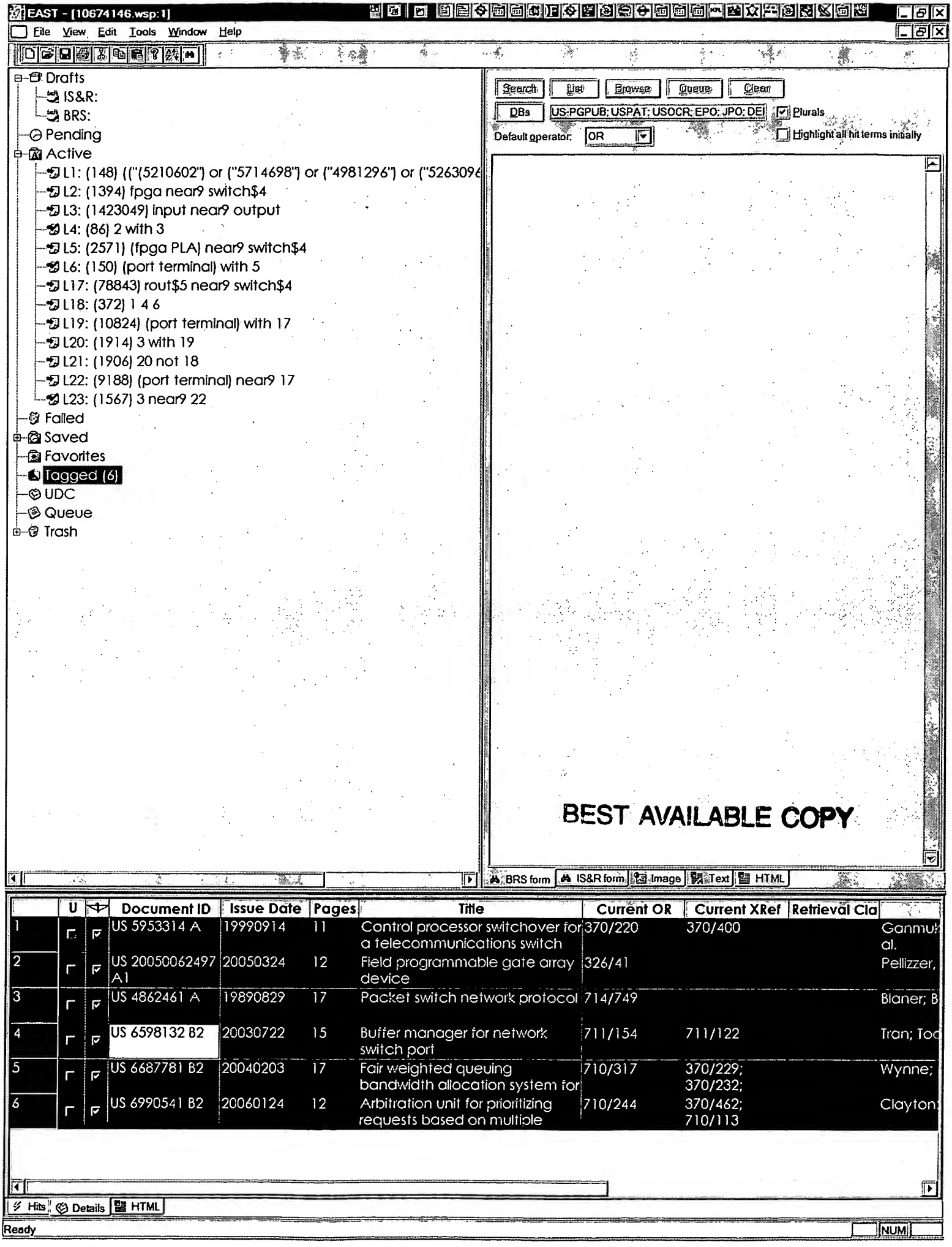
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L2: (1394) fpga near9 switch$4
L3: (1423049) input near9 output
L4: (86) 2 with 3
L5: (2571) (fpga PLA) near9 switch$4
L6: (150) (port terminal) with 5
L17: (78843) rout$5 near9 switch$4
L18: (372) 1 4 6
L19: (10824) (port terminal) with 17
L20: (1914) 3 with 19
L21: (1906) 20 not 18
L22: (9188) (port terminal) near9 17
L23: (1567) 3 near9 22
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BRS form IS&R form Image Text HTML
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Issue Date
Pages
Title
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Retrieval Cla
1 US 5953314 A 19990914 11 Control processor switchover for a telecommunications switch 370/220 370/400 Ganmu; al.
2 US 20050062497 A1 20050324 12 Field programmable gate array device 326/41 Pellizzer,
3 US 4862461 A 19890829 17 Packet switch network protocol 714/749 Blaner; B
4 US 6598132 B2 20030722 15 Buffer manager for network switch port 711/154 711/122 Tran; Toc
5 US 6687781 B2 20040203 17 Fair weighted queuing bandwidth allocation system for 710/317 370/229; 370/232; Wynne;
6 US 6990541 B2 20060124 12 Arbitration unit for prioritizing requests based on multiple 710/244 370/462; 710/113 Clayton
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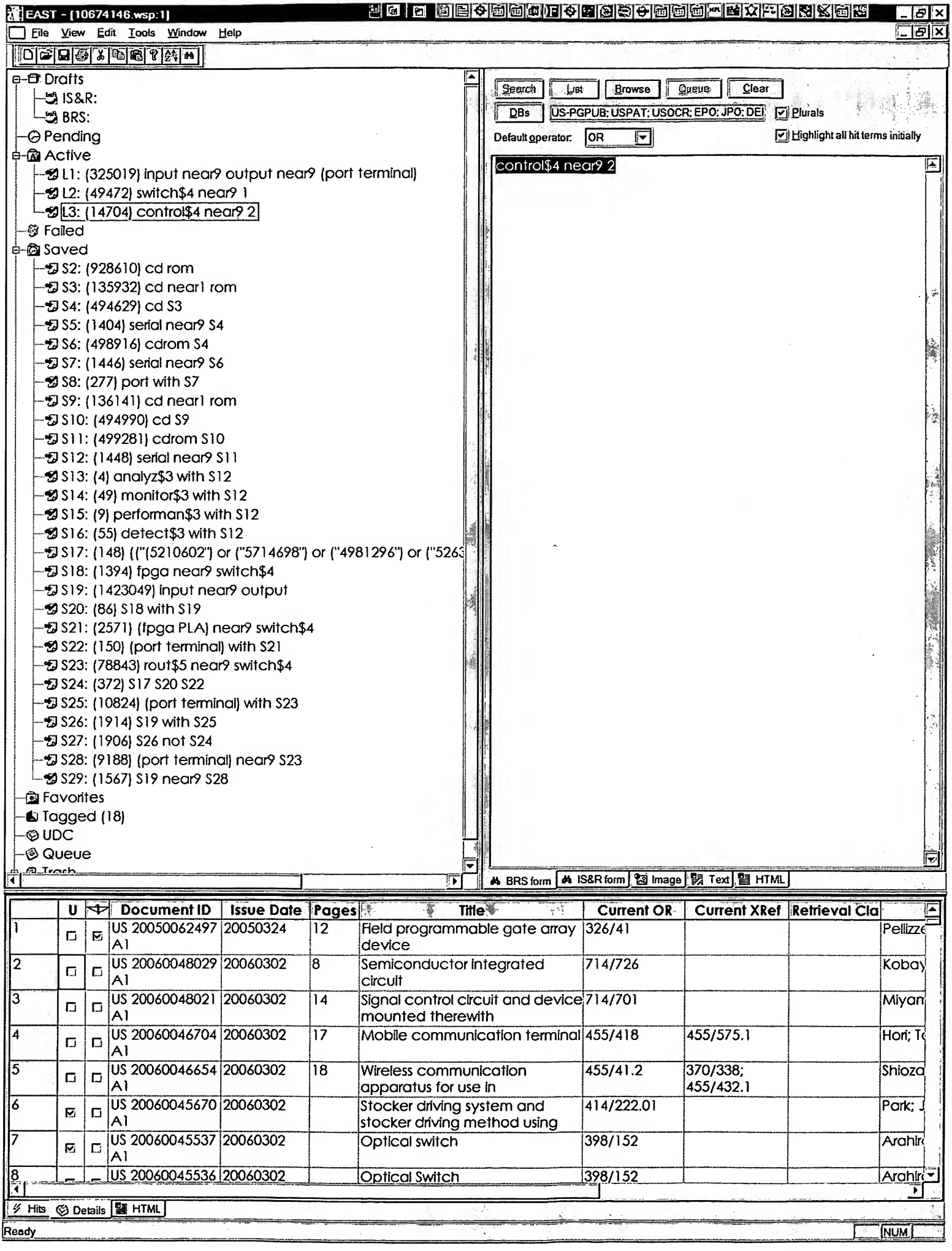

	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	
1	☐	☑	US 20050062497 A1	20050324	12	Field programmable gate array device	326/41			Pellizze
2	☐	☐	US 20060048029 A1	20060302	8	Semiconductor integrated circuit	714/726			Kobay
3	☐	☐	US 20060048021 A1	20060302	14	Signal control circuit and device mounted therewith	714/701			Miyam
4	☐	☐	US 20060046704 A1	20060302	17	Mobile communication terminal	455/418	455/575.1		Hori; T
5	☐	☐	US 20060046654 A1	20060302	18	Wireless communication apparatus for use in	455/41.2	370/338; 455/432.1		Shioza
6	☑	☐	US 20060045670 A1	20060302		Stocker driving system and stocker driving method using	414/222.01			Park; J
7	☑	☐	US 20060045537 A1	20060302		Optical switch	398/152			Arahir
8	☐	☐	US 20060045536	20060302		Optical Switch	398/152			Arahir

Hits Details HTML

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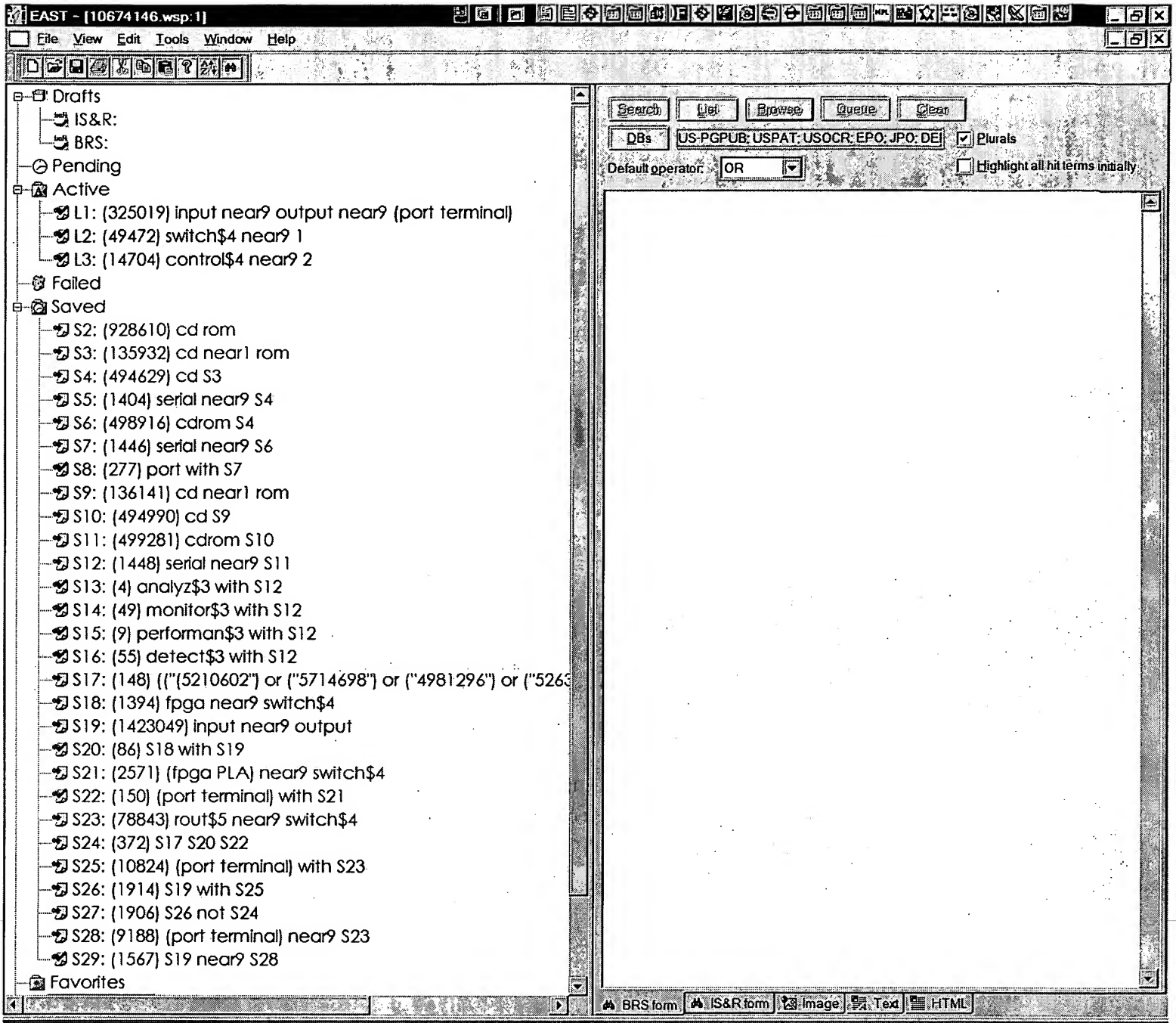

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	
3	☐	☑	US 6687781 B2	20040203	17	Fair weighted queuing bandwidt	710/317	370/229;		Wynne
4	☐	☑	US 20040083326	20040429	20	Switch scheduling algorithm	710/317			Wang
5	☐	☐	US 20010008001	20010712	35	Switching system and scramble	710/316	370/515;		Suemu
6	☐	☑	US 20040019732	20040129	21	Dual-role compatible USB hub d	710/313			Overt
7	☐	☑	US 6990541 B2	20060124	12	Arbitration unit for prioritizing req	710/244	370/462;		Clayto
8	☐	☑	US 20040103209	20040527	12	System and method for controlli	709/238			Kinosh
9	☐	☑	US 20020048280	20020425	22	Method and apparatus for load	370/468	370/412		Lee, E
10	☐	☑	US 20030123468	20030703	22	Apparatus for switching data in	370/412	370/413;		Nong,
11	☐	☑	US 20050201396	20050915	54	Separation of data and control i	370/401			Sindhu
12	☐	☑	US 20030227926	20031211	25	Method and system for guarant	370/395.42			Ramai
13	☐	☑	US 20050094644	20050505	54	Nonblocking and deterministic	370/395.4	370/415		Kondo
14	☐	☑	US 20040076154	20040422	34	Method and system for content	370/389	370/392		Mizuto
15	☐	☐	US 20040062238	20040401	16	Network switching device	370/360			Yoshiz
16	☐	☑	US 20020101865	20020801	34	Data transmission method and t	370/360	370/381;		Takag
17	☐	☑	US 5953314 A	19990914	11	Control processor switchover for	370/220	370/400		Ganm
18	☐	☑	US 20050062497	20050324	12	Field programmable gate array	326/41			Pellizze

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File View Edit Tools Window Help

- Active
  - L1: (325251) input near9 output near9 (port terminal)
  - L2: (49513) switch$4 near9 L1
  - L3: (14719) control$4 near9 L2
  - L4: (79) permi$5 near9 3
- Failed
- Saved
  - S2: (928610) cd rom
  - S3: (135932) cd near1 rom
  - S4: (494629) cd S3
  - S5: (1404) serial near9 S4
  - S6: (498916) cdrom S4
  - S7: (1446) serial near9 S6
  - S8: (277) port with S7
  - S9: (136141) cd near1 rom
  - S10: (494990) cd S9
  - S11: (499281) cdrom S10
  - S12: (1448) serial near9 S11
  - S13: (4) analyz$3 with S12
  - S14: (49) monitor$3 with S12
  - S15: (9) performan$3 with S12
  - S16: (55) detect$3 with S12
  - S17: (148) (("(5210602" or ("5714698") or ("4981296") or ("5263
  - S18: (1394) fpga near9 switch$4
  - S19: (1423049) input near9 output
  - S20: (86) S18 with S19
  - S21: (2571) (fpga PLA) near9 switch$4
  - S22: (150) (port terminal) with S21
  - S23: (78843) rout$5 near9 switch$4
  - S24: (372) S17 S20 S22
  - S25: (10824) (port terminal) with S23
  - S26: (1914) S19 with S25
  - S27: (1906) S26 not S24
  - S28: (9188) (port terminal) near9 S23
  - S29: (1567) S19 near9 S28
  - S30: (325019) input near9 output near9 (port terminal)
  - S31: (49472) switch$4 near9 S30
  - S32: (14704) control$4 near9 S31
- Favorites

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	
1	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	R	123/179.3;		MOSIE
2	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	M	123/179.3;		MOSIE
3	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	L	123/179.3;		MOSIE
4	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	I	123/179.3;		MOSIE
5	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	F02N11/08	123/179.3;		MOSIE
6	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	F02N	123/179.3;		MOSIE
7	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	EP	123/179.3;		MOSIE
8	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	CIPS	123/179.3;		MOSIE
9	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	CIPG	123/179.3;		MOSIE
10	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	CICL	123/179.3;		MOSIE
11	☐	☐	US 3543039 A	19701124	4	DELAY CIRCUIT FOR ENGINE ST	A	123/179.3;		MOSIE
12	☐	☐	US 3399271 A	19680827	9	Audience measuring system e	725/8	346/37;		ALEC
13	☐	☐	US 20020019983	20020214	97	Testing instrument	725/107	348/180		Emsley
14	☐	☐	US 4337533 A	19820629	25	Front loading type record playe	720/653	360/86;		Ando;
15	☐	☐	US 5127008 A	19920630	22	Integrated circuit driver inhibit c	714/726	714/724		Basset
16	☐	☐	US 20030182520	20030925	63	Control system, recording devic	711/154	711/167		Tsuner
17	☐	☐	US 20040039873	20040226	10	Management system for acces	711/105			Lin. Ho

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US006021115A

United States Patent [19]

Simpson et al.

[11] Patent Number: 6,021,115

[45] Date of Patent: Feb. 1, 2000

[54] **ATM SWITCH FLOW CONTROL**

[75] Inventors: **Robert Simpson**, Redland; **Neil Richards**, Cheddar; **Peter Thompson**, Newport, all of United Kingdom; **Pascal Moniot**, Bernin, France; **Marcello Coppola**, Trapani, Italy; **Pierre Dumas**, Sevres, France; **Thierry Grenot**, Clamart, France; **David Mouen Makoua**, Nanterre, France

[73] Assignee: **SGS-Thomson Microelectronics Limited**, Almondsbury Bristol, United Kingdom

[21] Appl. No.: 08/919,827

[22] Filed: Aug. 28, 1997

[30] Foreign Application Priority Data

Aug. 30, 1996 [GB] United Kingdom 9618132

[51] Int. Cl.[7] G08C 15/00

[52] U.S. Cl. 370/235; 370/253; 370/412

[58] Field of Search 370/229–232, 370/235–236, 253, 389, 390, 392, 410–418, 468, 395

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,166,926 11/1992 Cisneros et al. 370/60

OTHER PUBLICATIONS

Serving Humanity Through Communications, Supercomm/ICC, May 1–5, 1994 vol. 1, No. _, IEEE, pp. 402–409, Fan et al, Expandable Atom Switch Architecture (XATOM) for ATM Lans, p. 404–407.

Standard Search Report dated Nov. 29, 1996.

IEEE Transactions on Communications, vol. 41, No. 1, Jan. 1, 1993, pp. 237–245 Noboru Endo, Shared Buffer Memory Switch for an ATM Exchange, p. 238, 239.

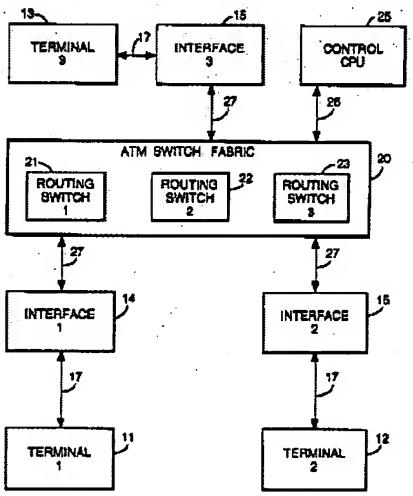
Serving Humanity Through Communications, Supercomm/ICC, May 1–5, 1994 vol. 1, No. —, May 1, 1994 IEEE pp. 402–409 Fan R et al., Expandable Atom Switch Architecture (XATOM) for ATM Lans p. 404, 407.

Primary Examiner—Chi H. Pham
Assistant Examiner—Maikhanh Tran
Attorney, Agent, or Firm—Wolf, Greenfield & Sacks, P.C.

[57] **ABSTRACT**

A network of ATM routing switches transmits digital signal cells of a first type requiring integrity of transmission and a second type accepting some loss in transmission, each switch has buffer circuitry. a plurality of output ports each having a plurality of queues of cells awaiting output, each output port having control circuitry to provide in an output frame control bits indicating the type of cell, a path identifier and the existence of flow congestion at the routing switch which it outputting the frame, thereby inhibiting transmission of further frames to that location until a frame is received from that location indicating that the congestion is cleared.

17 Claims, 16 Drawing Sheets



designation only to an input port of a connected switch having a compatible designation.

Claims Text - CLTX (7):
7. A network according to claim 1 in which each switch includes designation circuitry to provide a respective designation to each input port, which is used to determine permitted paths to avoid deadlock in the network, each cell which is input having the designation of the respective input port, said control circuitry being responsive to said designations to output to a connected input of a further switch in the network only cells of a designation compatible with the designation of said connected input.

Claims Text - CLTX (16):
16. A method according to claim 9 including providing a respective designation to each input port on each switch, which designation is used to determine permitted paths to avoid deadlock in the network, each cell which is input having the designation of the respective input port, and operating said control circuitry to output a cell of any given designation only to an input port of a connected switch having a compatible designation.

Details | Text | Image | HTML | Full

	U	1	Documen	Issue D	Pa	Current	Current	Title
25	☐	☐	US 50509	199109	7	385/17	385/24	Optical matrix switch wi
26	☐	☐	US 50489	199109	10	385/17	385/24	Optical matrix switch fc
27	☐	☐	US 20040	200410	13	385/16		Optical switching devic
28	☐	☐	US 69344	200508	15	385/16	385/24	Circuit for switching on
29	☐	☐	US 20050	200509	18	385/14	385/16	Opto-electronic integra
30	☐	☐	US 20030	200306	21	380/201		MPEG data recorder h
31	☐	☐	US 48948	199001	8	379/390	330/290	Signal compression cir
32	☐	☐	US 52552	199310	8	370/416		Controller for input-que
33	☐	☐	US 60211	200002	27	370/235	370/253	ATM switch flow contro

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